# ANNA UNIVERSITY <br> MODEL QUESTION PAPER <br> B.E / B.Tech. Degree Examinations 

## IF 242 DIGITAL SYSTEM DESIGN

## PART - A

( $10 \times 2$ = 20 Marks)

1. List the first 16 numbers in base 12 . Use the letters $A$ and $B$ to represent the last two digits. Convert the numbers (546)12 to base 8 .
2. Using DeMorgan's theorem, convert the following Boolean expression to an equivalent expression that has only OR and complement operations. Show that the function can be implemented with logic circuits that have only OR gates and inverters:

$$
\mathrm{F}=\left(\mathrm{y}+\mathrm{z}^{\prime}\right)(\mathrm{x}+\mathrm{y})\left(\mathrm{y}^{\prime}+\mathrm{z}\right)
$$

3. A combinational switching network has 4 inputs (A, B, C, D) and one output F. $F=0$ if 3 or 4 of the inputs are 0 .

- Write the maxterm expansion for $F$.
- Using AND and OR gates, find a minimum three-level network to realize F .

4. What do you mean by positive logic, negative logic and mixed logic?
5. Realize the operation of a full adder using a $3 \times 8$ decorder.
6. Implement the following function with a multiplexer:
$\mathrm{F}(\mathrm{A}, \mathrm{B}, \mathrm{C}, \mathrm{D})=\sum(0,1,3,4,8,9,15)$
Use $B, C$ and $D$ as select lines.
7. With the help of a block diagram, explain the operation of a J-K Master-Slave Flip flop.
8. Draw the logic diagram of a D Flip-flop using NAND gates and derive its characteristic table.
9. What are the guidelines to be followed while making state assignments?
10. What are hardware description languages?

PART - B
( $5 \times 16$ = 80 Marks)
11. i) In what way is the Quine-McCluskey method advantages over the Karnaugh method of simplifying a Boolean function?
ii) Simplify the given Boolean function using Quine-McClukey, method:

$$
\sum(\mathrm{w}, \mathrm{x}, \mathrm{y}, \mathrm{z})=\sum(1,4,6,7,8,9,10,11,15)
$$

12a. i) Which are functionally complete sets of logic gates? Explain.
ii) How are AND, OR and NOT operations realized with NAND gates?

Using AND and OR gates, find a minimum network to realize
$\mathrm{f}(\mathrm{a}, \mathrm{b}, \mathrm{c}, \mathrm{d})=\mathrm{M} 1 \mathrm{M} 2 \mathrm{M} 5 \mathrm{M} 9 \mathrm{M} 10 \mathrm{M} 14$ using two-level logic and three-level logic.
(OR)
12b. i) Convert the following network to all NAND gates, by adding bubbles and inverters where necessary.
ii) Convert to all NOR gates.


13a. i) Discuss the usage of multiplexers in digital systems.
ii) Explain with the help of a block diagram, a quadruple 2-to-1 line multiplexer.
(OR)
13b. Realize the functions given below using a PLA. Give the PLA table and internal connection diagram for the PLA:

$$
\begin{aligned}
& \text { F1 (a,b,c,d) }=\sum(1,2,4,5,6,8,10,12,14) \\
& \text { F2 }(\mathrm{a}, \mathrm{~b}, \mathrm{c}, \mathrm{~d})=\sum(2,4,6,8,10,11,12,14,15)
\end{aligned}
$$

14a. Design a counter which counts the following sequence:

$$
0,8,12,10,14,19,13,11,15,0,8,12, \ldots
$$

Use clocked J-K flip flops and NAND gates.
(OR)
14b. i) Specify the method that is used to construct a state table.
ii) Describe with suitable examples, the two types of clocked-sequential networks.

15a. i) What is an SM chart? In what way is it different from an ordinary flow chart?
ii) Derive the SM chart for a binary multiplier control and explain the sequences indicated in the chart.
(OR)
15b. i) Describe with suitable examples, the different conditions that can occur in a network.
ii) With suitable examples, explain the hazards in combinational networks.

## CS 233 - SYSTEM SOFTWARE

$$
\text { PART A }-(10 \times 2=20 \text { marks })
$$

1. Define System Software.
2. Illustrate how input and output operations are performed in SIC.
3. Compare assembler and compiler.
4. List the types of assemblers.
5. What is a loader?
6. Give an example of data shared between PES.
7. Define macro.
8. What is conditional macro expansion?
9. List the various phases of a compiler.
10. What is debugging?

$$
\text { PART B }-(5 \times 16=80 \text { marks })
$$

11. Write short notes on System Software tools with examples.
12. (a) Explain the various instruction formats provide atleast 3 examples for each.

Or
(b) Explain addressing modes in detail.
13. (a) Explain machine dependent assembler features.

Or
(b) Explain Assembler design options in detail.
14. (a) Explain Dynamic linking in detail.

Or
(b) Write short notes on machine independent loader features.
15. (a) Explain different types of linkers.

Or
(b) Explain the implementation of text editors in detail.

## CS 234 - DATABASE MANAGEMENT SYSTEM

$$
\text { PART A }-(10 \times 2=20 \text { marks })
$$

1. Distinguish between physical and logical data independence.
2. What is a data dictionary? What are the informations stored in the data dictionary?
3. What is a view and how is it created? Explain with an example.
4. In what way is an Embedded SQL different from SQL? Discuss.
5. Which condition is called referential integrity? Explain its basic concepts.
6. Explain with a simple example, the lossless-join decomposition.
7. How to choose the best evaluation plan for a query? Explain.
8. What is a timestamp-ordering scheme? Specify two simple methods for implementing this scheme.
9. Give a comparison of object-oriented and object-relational databases.
10. Which are the two models used for discovering rules from database? Give the general form of rules to express knowledge.

PART B - $(5 \times 16=80$ marks $)$
11. (i) What are data models and how are they grouped?
(ii) Explain in detail any two data models with sample databases.
12. (a) (i) Discuss the fundamental operations in the relational algebra.
(ii) For each operation give an example.

## Or

(b) (i) SQL language has several parts. What are they?
(ii) How many clauses are there in the basic structure of an SQL? Explain.
13. (a) (i) Discuss the various pitfalls in a relational database design using a sample database.
(ii) Explain at least two of the desirable properties of decomposition.

Or
(b) (i) What are the merits and demerits of a $\mathrm{B}+$ tree index structure?
(ii) Describe the structure of a B+ tree.
(iii) How update operations are performed on $\mathrm{B}+$ trees?
14. (a) With the help of a neat diagram, explain the basic steps involved in processing a query.

Or
(b) (i) What are the different types of storage media?
(ii) Explain with a diagram, the block storage operations.
15. (a) (i) Draw a neat sketch to indicate the architecture of a distributed system.
(ii) Explain the basic failure types in a distributed environment.
(iii) Diagramatically represent the network topology used in a distributed system and explain the advantages and disadvantages of each configuration.

Or
(b) (i) Explain the architecture of a data warehouse with a neat diagram.
(ii) What are the various issues to be considered while building a warehouse? Explain.

## EE 255 - ELECTRICAL ENGINEERING AND CONTROL SYSTEMS <br> PART A - $(10 \times 2=20$ marks $)$

1. State superposition theorem.
2. Give the algorithm for solving Loop Current Analysis.
3. Draw the equivalent circuit of a single phase transformer and name the components.
4. Draw Torque Versus armature current characteristics of D.C. shunt and series motors.
5. Explain briefly why single phase induction motor is not self starting.
6. Draw the circuit diagram of three phase rectifier using SCRs.
7. Show that the transfer function of canonical form of general block diagram with negative feed back is given by

$$
G(s) /(1+G(s) \cdot H(s))
$$

8. State Mason's rule.
9. What is the need for state variable approach?
10. Give steady state error for step and velocity input.

$$
\text { PART B }-(5 \times 16=80 \text { marks })
$$

11. A $10 \mathrm{kVA}, 200 / 400 \mathrm{~V}, 50 \mathrm{~Hz}$, single phase transformer gave the following test results. Open circuit test (hV winding open) $200 \mathrm{~V}, 1.3 \mathrm{~A}, 120 \mathrm{~W}$.

Short circuit test (lv winding short circuited) $22 \mathrm{~V}, 30 \mathrm{~A}, 200 \mathrm{~W}$.
12. Calculate (i) magnetising current and the current corresponding to core loss at normal voltage and frequency (ii) parameters of equivalent circuit as referred to low voltage winding.
(a) For the circuit shown in Fig. 12 (a), find the currents through $R_{3}$ and $R_{4}$.
$E_{a}=100 \mathrm{~V} ; E_{b}=40 \mathrm{~V} ; R_{1}=R_{2}=R_{5}=10 \mathrm{ohms}$
$R_{3}=R_{4}=20$ ohms.


Fig. 12 (a)

## Or

(b) Two similar coils are magnetically coupled and their coefficient of coupling is 0.3 . When the two are cumulatively connected in series, the total inductance is 100 mH . Calculate (i) self inductance of each coil (ii) total inductance when the coils are connected in series opposing connection (iii) the energy in the magnetic field with a current of 3 A and the two coils connected in both series aiding and series opposing connections.
13. (a) (i) Derive the torque equation of a d.c. motor.
(ii) A 220 V shunt motor with an armature resistance of 0.5 ohm is excited to give constant field. At full load, the speed is 500 RPM and armature current is 30 A . If a resistance of 1 ohm is connected in series with the armature find the speed at full load torque.

## Or

(b) Explain double field revolving theory applied to single phase induction motor and develop the equivalent circuit.
14. (a) (i) Explain the principle of operation of a shaded pole motor.
(ii) Draw and explain the working of $\mathrm{Mc}-$ Murray inverter.

Or
(b) (i) Briefly explain open loop, closed loop and automatic control system.
(ii) Using Mason's rule, determine the transfer function of the signal flow graph shown in Fig. 14 (b).


Fig. 14 (b)
15. (a) Obtain the state model of the electromechanical system shown in Fig. 15 (a).


Fig. 15 (a)
Or
(b) (i) Explain time response specifications.
(ii) A unity feed back system has the forward open loop transfer function $G(s)=\frac{10}{s+1}$. Find the steady state error and the generalised error coefficients for $r(t)=t$.

$$
\begin{gathered}
\text { MA } 231 \text { Mathematics III } \\
\text { Part }- \text { A ( } 10 \times 2=20 \text { Marks })
\end{gathered}
$$

1. Form a partial differential equation by eliminating the arbitrary function $\phi$ from $z=(x+y) \phi\left(x^{2}-y^{2}\right)$.
2. Find the complete integral of $q=2 p x$.
3. Find the half range sine series for $\mathrm{f}(\mathrm{x})=2$ in $0<\mathrm{x}<4$.
4. If the cosine series for $\mathrm{f}(\mathrm{x})=\mathrm{x} \sin \mathrm{x}$ for $0<\mathrm{x}<\pi$ is given by
$x \sin x=1-\frac{1}{2} \cos x-2 \sum_{n=2}^{\infty} \frac{(-1)^{n}}{n^{2}-1} \cos n x$, show that
$1+2\left[\frac{1}{1.3}-\frac{1}{3.5}+\frac{1}{5.7}-\ldots \ldots \ldots.\right]=\frac{\pi}{2}$.
5. Classify the partial differential equation

$$
\left(1-x^{2}\right) z_{x x}-2 x y z_{x y}+\left(1-y^{2}\right) z_{y y}+x z_{x}+3 x^{2} y z_{y}-2 z=0
$$

6. The steady state temperature distribution is considered in a square plate with sides $\mathrm{x}=0, \mathrm{y}=0, \mathrm{x}=\mathrm{a}$ and $\mathrm{y}=\mathrm{a}$. The edge $\mathrm{y}=0$ is kept at a constant temperature T and the other three edges are insulated. The same state is continued subsequently. Express the problem mathematically.
7. Find the Laplace transform of $\frac{e^{-t}-e^{-3 t}}{t}$.
8. Verify the initial value theorem for $f(t)=5+4 \cos 2 t$.
9. If Fourier transform of $f(x)$ is $F(s)$, prove that the Fourier transform of $f(x) \cos a x$ is $\frac{1}{2}[F(s-a)+F(s+a)]$.
10. Find the Fourier cosine integral representation of $f(x)=\left\{\begin{array}{cc}1, & 0<x<1 \\ 0, & x>1\end{array}\right.$.

$$
\text { Part - B ( } 5 \times 16=80 \text { Marks })
$$

Question No. 11 has no choice; Questions 12 to 15 have one choice (either - or type) each.
11. (i) Expand in Fourier series of periodicity $2 \pi$ off $(x)=\left\{\begin{array}{cc}x & \text { if } 0<x<\pi \\ 2 \pi-x & \text { if } \pi<x<2 \pi\end{array}\right.$.
(ii) Find the half-range cosine series for the function $f(x)=x, 0<x<\pi$ and hence deduce the sum of the series $\sum_{n=0}^{\infty} \frac{1}{(2 n+1)^{4}}$.
12. (a) (i) Find the complete solution and singular solution of $z=p x+q y+p 2-q 2$.
(ii) Find the general solution of $x\left(z^{2}-y^{2}\right) p+y\left(x^{2}-z^{2}\right) q=z\left(y^{2}-x^{2}\right)$.
(OR)
(b) (i) Solve: $\left(D^{2}-4 D^{\prime 2}\right) z=\cos 2 x \operatorname{coa} 3 y$.
(ii) Solve : $\left[\left(D+D^{\prime}-1\right)\left(D+2 D^{\prime}-3\right)\right] z=4+3 x+6 y+e^{x+y}$.
13. (a) A taut string of length $L$ is fastened at both ends. The midpoint of the string is taken to a height of b and then released from rest in this position. Find the displacement of the string at any time $t$.
(OR)
(b) A rod 30 cm long, has its ends A and B at $20^{\circ} \mathrm{C}$ and $80^{\circ} \mathrm{C}$ respectively, until steady state conditions prevail. The temperature at the end $B$ is then suddenly reduced to $60^{\circ} \mathrm{C}$ and at the end A is raised to $40^{\circ} \mathrm{C}$ and maintained so. Find the resulting temperature $u(x, t)$.
14. (a) (i) Find the Laplace transform of the function

$$
f(t)=\left\{\begin{array}{cc}
\sin t, & 0<t<\pi \\
0, & \pi<t<2 \pi
\end{array}\right.
$$

and extending periodically with period $2 \pi$.
(ii)Apply the Convolution theorem to find $L^{-1}\left(\frac{s}{\left(s^{2}+9\right)\left(s^{2}+125\right)}\right)$.
(b) (i) Solve by using Laplace transform technique, $y^{\prime \prime}+3 y^{\prime}+2 y=2\left(t^{2}+t+1\right)$, given that $\mathrm{y}(0)=2$ and $\mathrm{y}^{\prime}(0)=0$.
(ii) Find the inverse Laplace transform of $\frac{4(s-1)}{\left(s^{2}+2 s+7\right)^{2}}$.
15. (a) (i) Find the Fourier transform of $f(x)=\left\{\begin{array}{cc}1-|x| & \text { for }|x| \leq 1 \\ 0 & \text { for }|x|>1\end{array}\right.$.

Hence evaluate the following integral:
(ii) $\int_{0}^{\infty}\left(\frac{\sin x}{x}\right)^{2} d x$.
(iii) $\int_{0}^{\infty}\left(\frac{\sin x}{x}\right)^{4} d x$.

## (OR)

(b) (i) Find the Fourier sine and cosine transform of $e^{-2 x}$.

Hence find the value of the following integrals:
(ii) $\int_{0}^{\infty} \frac{d x}{\left(x^{2}+4\right)^{2}}$.
(iii) $\int_{0}^{\infty} \frac{x^{2} d x}{\left(x^{2}+4\right)^{2}}$.

## CS 232 — DIGITAL SYSTEMS

PART A - $(10 \times 2=20 \mathrm{marks})$

1. Find the hexadecimal equivalent of the octal number 153.4.
2. Show that the excess -3 code is self-complementing.
3. State and prove Demorgan's theorem.
4. Show that a positive logic NAND gate is the same as a negative logic NOR gate.
5. Distinguish between a decoder and a demultiplexer.
6. Derive the characteristic equation of a JK flip-flop.
7. State the relative merits of series and parallel counters.
8. What are Mealy and Moore machines?
9. A shift register comprises of JK flip-flops. How will you complement the contents of the register?
10. What is a dynamic hazard?

PART B - $(5 \times 16=80$ marks $)$
11. (i) Explain how you will construct an $(\mathrm{n}+1)$ bit Gray code from an n bit Gray code.
(ii) Determine the MSP form of the switching function $F=\Sigma(0,1,4,5,6$, $11,14,15,16,17,20-22,30,32,33,36,37,48,4952,53,59,63)$
12. (a) Implement the switching function whose octal designation is 274 using NOR gates only.

Or
(b) Design a switching circuit that converts a 4 bit binary code into a 4 bit Gray code using ROM array.
13. (a) Implement a binary serial adder using an SRFF programmable logic array.

> Or
(b) Using D flip-flops, design a synchronous counter which counts in the sequence.
$000,001,010,011,100,101,110,111,000$.
14. (a) (i) Convert the following mealy machine into a Moore machine :

|  | Ns, Z |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| x1 x2 |  |  |  |  |
| PS | 00 | 01 | 11 | 10 |
| A | A, 0 | A, 1 | B, 0 | A, 1 |
| B | A 1 | B, 0 | B 1 | B, 0 |

(ii) Minimise the following state table:

|  | $\begin{gathered} \text { Ns, Z } \\ \mathrm{x} \end{gathered}$ |  |
| :---: | :---: | :---: |
| PS | 0 | 1 |
| A | A, 0 | D, 1 |
| B | C, 1 | D, 0 |
| C | B, 0 | E, 1 |
| D | D, 1 | A, 1 |
| E | E, 0 | G, 1 |
| F | G, 0 | E, 0 |
| G | D, 1 | A, 1 |
| H | D, 1 | C, 1 |

Use Paull and Unger's implication chart.
Or
(b) Using JK flip-flops, design a synchronous sequential circuit having one input and one output. The output of the circuit is a 1 whenever three consecutive 1's are observed. Otherwise the output is zero.
15. (a) Implement the switching function $F=\Sigma(0,1,3,4,8-12)$ by a static hazard free two level OR-AND gate network.

Or
(b) Show that no static 0 (static 1) hazard can happen in a two level AND-OR (OR-AND) realisation of a switching function F .

